IN THE CLAIMS:

1-8 (Canceled).

9. (Currently Amended) A memory controller for controlling a memory having a plurality of banks, the memory controller comprising:

an arbitration circuit for arbitrating a memory access request from a plurality of blocks for accessing a memory, wherein bank access data is access data to the memory with a predetermined number of bytes for writing or reading on a same bank of the memory and block access data is a data unit with a pair of bank access data including a first-half bank access data and a second-half bank access data belonging to different banks, the arbitration circuit comprising:

a request receiving block for receiving a block access data and determining a change in an order of memory access if a second-half bank access data of a block access data where memory access is permitted immediately before is the same as a first-half bank access data of a block access data of a subsequent memory access request;

an enabling signal generation block, which is instructed by the request receiving block, for generating an enabling signal and outputting the enabling signal to a block permitted to access the memory; and

a control signal generation block, which is instructed by the request receiving block, for generating a control signal;

a command generation block for generating a memory command for ~~a~~ the memory based on ~~a~~ the control signal from the arbitration circuit;

an address generation block for receiving a memory address from a block permitted to access by the arbitration circuit and for outputting a memory address to the memory; and

a data latch block for latching either write data from the block permitted by the arbitration circuit for accessing a memory or read data from a memory and passing data between a memory and the block, the data latch block comprising:

a write data latch block for receiving and latching write data from the plurality of blocks;

a read data latch block for receiving and latching read data read from the memory; and

a data change block for either changing an order of bank access data outputted by the write data latch block and outputting data as write data to the memory, or changing an order of bank access data outputted by the read data latch block and outputting data as read data to a block permitted to perform read access to the memory,

wherein the data change block is controlled based on a data latch control signal from the arbitration circuit indicating a change in the order of memory access of the first-half and second-half bank access data in the block access data.

~~bank access data is access data to the memory comprising a predetermined number of bytes for performing writing or reading on a same bank of the memory, block access data is a data unit comprising two sets of the bank access data belonging to different banks, and if the plurality of blocks make a memory access request for each piece of the block access data, when a second-~~

~~half-bank where memory access is permitted immediately before is the same as the first half bank of a subsequent memory access request, the arbitration circuit changes an order of memory access of the bank access data in the block access data,~~

~~wherein the data latch block comprises:~~

~~a write data latch block for receiving and latching write data from the plurality of blocks;~~

~~a data change block for changing, based on a data latch control signal from the arbitration circuit, an order of bank access data outputted by the write data latch block, outputting the data as write data to the memory changes an order of bank access data outputted by a read data latch block, and outputting the data as read data to a block permitted to perform read access to the memory; and~~

~~a read data latch block which receives and latches the read data having been read from the memory.~~

10. (Currently Amended) The memory controller according to claim 9, wherein the arbitration circuit further comprises:

~~a request receiving block for receiving a memory request and a memory address from the plurality of blocks, the request receiving block comprising a bank decision unit for deciding, based on the received memory address, whether access is made to the same bank regarding a second half bank where memory access has been permitted immediately before and a first half bank of a subsequent memory access request, and providing an instruction to generate an enabling signal;~~

a memory access priority designating unit for designating priority of memory access from the plurality of ~~blocks;~~ blocks.

~~an enabling signal generation block which is instructed by the request receiving block, for generating the enabling signal and outputting the enabling signal to the block permitted to access the memory; and~~

~~a control signal generation block, which is instructed by the request receiving block, for generating the control signal.~~

11. – 12. (Canceled).

13. (Previously Presented) The memory controller according to claim 10, wherein the memory access priority designating unit is set from outside and the priority of access from the plurality of blocks to the memory is changed according to a setting of the memory access priority designating unit.

14. (Original) The memory controller according to claim 9, wherein the memory is a synchronous memory.

15. (Currently Amended) A memory controller for controlling a memory having a plurality of banks, the memory controller comprising:

an arbitration circuit for arbitrating a memory access request from a plurality of blocks for accessing a ~~the memory;~~ memory, wherein the plurality of blocks comprises a block for making

a memory access request, block access data is a data unit comprising a pair of bank access data belonging to different banks, and a memory request is made by a single bank access data from a block permitted to access the memory, the arbitration circuit comprising:

a request receiving block for receiving memory requests from the plurality of blocks, the request receiving block comprising a data unit decision unit for deciding whether a data unit of requested memory access based on the received memory request is a data unit comprising two sets of the bank access data or the bank access data alone, and instructing the command generation block to provide a wait cycle when a memory access request is made by the bank access data alone from the block permitted to access the memory;

a wait cycle designating unit for designating the number of wait cycles provided when memory access is requested from the plurality of blocks by the bank access data alone;

an enabling signal generation block which is instructed by the request receiving block for generating the enabling signal and outputting the enabling signal to the block permitted to access the memory; and

a control signal generation block which is instructed by the request receiving block for generating the control signal and generates each control signal;

a command generation block for generating a memory command for a memory based on a control signal from the arbitration circuit;

an address generation block for receiving a memory address from a block permitted by the arbitration circuit for accessing a memory and outputting the memory address to such memory; and

a data latch block for latching either write data from the block permitted by the arbitration circuit for accessing a memory or read data from a memory and passing data between a memory and the block~~;~~

~~wherein~~

~~bank access data is access data to the memory comprising a predetermined number of bytes for performing writing or reading on a same bank of the memory, block access data is a data unit comprising two sets of the bank access data belonging to different banks, and the arbitration circuit instructs the command generation block to provide a wait cycle when a memory access request is made by the bank access data alone from the block permitted to access the memory~~.

16. (Currently Amended) The memory controller according to claim 15, wherein the arbitration circuit further comprises:

~~a request receiving block for receiving a memory request and a memory address from the plurality of blocks, the request receiving block comprising a data unit decision unit for deciding a data unit of requested memory access based on the received memory request, and providing an instruction to generate an enabling signal;~~

a memory access priority designating unit for designating priority of memory access from the plurality of ~~blocks;~~ blocks.

~~a wait cycle designating unit for designating the number of wait cycles provided when memory access is requested from the plurality of blocks by the bank access data alone,~~

~~an enabling signal generation block which is instructed by the request receiving block, for generating the enabling signal and outputting the enabling signal to the block permitted to access the memory; and~~

~~a control signal generation block, which is instructed by the request receiving block, for generating the control signal.~~

17. (Previously Presented) The memory controller according to claim 16, wherein the memory access priority designating unit is set from outside and the priority of access from the plurality of blocks to the memory is changed according to a setting of the memory access priority designating unit.

18. (Currently Amended) The memory controller according to claim ~~16,~~ 15, wherein the wait cycle designating unit is set from outside and the number of wait cycles provided by the command generation block is changed according to a setting of the wait cycle designating unit.

19. (Previously Presented) The memory controller according to claim 15, wherein the memory is a synchronous memory.

20-33 (Canceled).

34. (Currently Amended) A memory controller for controlling a memory having a plurality of banks, the memory controller comprising:

an arbitration circuit for arbitrating a memory access request from a plurality of blocks for accessing a ~~the~~ memory, the arbitration circuit comprising:

a bank decision unit for receiving a memory address from the plurality of blocks and deciding whether access is made to the same bank or not based on the received memory address;

an access request decision unit for receiving a memory requ4st from the plurality of blocks and deciding the kind of requested memory access based on the received memory request;

a request receiving block comprising the bank decision unit and the access request decision unit for providing an instruction to generate an enabling signal;

a memory access priority designating unit for designating the priority of memory access from the plurality of blocks;

an arbitrating method designating unit for designating either higher priority on a bank changing the priority of memory access to prevent successive access to the same bank or higher priority on access changing the priority of memory access to have successive read access when the memory access request from the plurality of blocks is made to the same bank as immediately preceding access and memory access permitted by the arbitration circuit immediately before is read access;

an identical bank priority designating unit for selecting a block to be subsequently permitted to access when the arbitrating method designating unit is set so as to place higher priority on a bank;

a read access priority designating unit for selecting a block to be subsequently permitted to perform read access when the arbitrating method designating unit is set so as to place higher priority on access;

an enabling signal generation block which is instructed by the request receiving block for generating the enabling signal for outputting the enabling signal to the block permitted to access the memory; and

a control signal generation block which is instructed by the request receiving block for generating the control signal for generating each control signal;

a command generation block for generating a memory command for a memory based on a control signal from the arbitration circuit;

an address generation block for receiving a memory address from a block permitted by the arbitration circuit for accessing a memory and outputting the memory address to such memory; and

a data latch block for latching either write data from the block permitted by the arbitration circuit for accessing a memory or read data from a memory and passing data between a memory and the block;

~~wherein the arbitration circuit designates an arbitrating method for changing priority of memory access from the plurality of blocks when the memory access request from the plurality~~

~~of blocks is made to the same bank as immediately preceding access and memory access permitted by the arbitration circuit immediately before is read access~~.

35. (Canceled)

36. (Currently Amended) The memory controller according to claim ~~35,~~ 34, wherein the memory access priority designating unit is set from outside and the priority of access from the plurality of blocks to the memory is changed according to a setting of the memory access priority designating unit.

37. (Currently Amended) The memory controller according to claim ~~35,~~ 34, wherein the arbitrating method designating unit is set from outside and the arbitrating method of memory access from the plurality of blocks is changed according to a setting of the arbitrating method designating unit.

38. (Currently Amended) The memory controller according to claim ~~35,~~ 34, wherein the identical bank priority designating unit is set from outside and a block to be subsequently permitted to access to the memory is selected according to priority set by the identical bank priority designating unit when the arbitrating method designating unit is set so as to place higher priority on a bank and a memory access request is made from the plurality of blocks to the same bank as immediately preceding access.

39. (Currently Amended) The memory controller according to claim ~~35,~~ 34, wherein the read access priority designating unit is set from outside and a block to be subsequently permitted to perform read access to the memory is selected according to priority set by the read access priority designating unit when the arbitrating method designating unit is set so as to place higher priority on access and memory access permitted by the arbitration circuit immediately before is read access.

40. (Original) The memory controller according to claim 34, the memory is a synchronous memory.